METHOD OF CHEMICAL MODIFICATION OF STRUCTURE TOPOGRAPHY

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BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates generally to methods of thin film deposition and, more specifically, to a

10 method of minimizing structure overhang during the process of filling high aspect ratio gaps on substrates.

Background of the Invention

15 As semiconductor technology advances, circuit elements and interconnections on wafers or silicon substrates become increasingly more dense. In order to prevent unwanted interactions between these circuit elements, insulator-filled gaps or trenches located

20 therebetween are provided to physically and electrically isolate the elements and conductive lines. However, as circuit densities continue to increase, the widths of these gaps decrease, thereby increasing gap aspect ratios, typically defined as the gap height

25 divided by the gap width. As a result, filling these narrower gaps becomes more difficult, which can lead to unwanted voids and discontinuities in the insulating or gap-fill material.

In previous generations of microelectronic devices

30 the gaps between metal lines were filled using either PECVD (plasma enhanced chemical vapor deposition) processes or the combinations of those with sputter etch steps. For example, U.S. Patent No. 5,270,264 to Andideh et al. describes a gap-filling process which

involves the steps of deposition by PECVD, followed by argon sputter etching, followed by another PECVD deposition step, i.e., a PECVD "dep-etch-dep" process. The article by S. Pennington et al. (hereinafter "the

5   article by Pennington et al."), entitled "An Improved Interlevel Dielectric Process for Submicron Double-Level Metal Products," in *Proceedings of the 6th International IEEE VLSI Multilevel Interconnection Conference*, (1989), pp. 355-359, describes a dielectric

10 gap-filling process using both PECVD and thermal CVD (THCVD). The article by D. Cote et al. (hereinafter "the article by Cote et al."), entitled "Low-Temperature Chemical Vapor Deposition Processes and Dielectrics for Microelectronic Circuit Manufacturing

15 at IBM", in the *IBM Journal of Research and Development*, vol. 39, no. 4, (July 1995), pp. 437-464, describes several known CVD processes, including low pressure (LP), atmospheric pressure (AP) CVD, and plasma-enhanced (PE) CVD, which are background to the

20 present invention. However, the gap-fill capabilities of such processes or combinations of processes do not extend beyond aspect ratios of 1.3:1 at spacing 0.45 μm or 4500 Å, even when "dep-etch-dep" cycles are performed, as described in U.S. Patent 5,270,264 and

25 the article by Cote et al. Specifically, the article by Cote et al. refers to and presents data demonstrating the inability of PECVD processes to satisfy the gap-fill requirements of advanced microelectronic devices with either undoped or doped

30 silica glass.

    In the gap-fill process described in U.S. Patent No. 5,270,264, a step of deposition by PECVD is followed by a sputter etch step with argon and another

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step of deposition by PECVD. As understood by those skilled in the art, deposition by PECVD is strictly a deposition step, i.e., not involving simultaneous etching during exposure to the depositing plasma. U.S.

5   Patent No. 5,270,264 describes a gap-filling process which performs a sputter etch using inert gases of heavy atomic weight such as Ar, Kr, and Xe. The process parameters for the PECVD deposition and etching are specified in that patent for the plasma power

10   density and pressure. In addition, the capabilities of the dep-etch-dep processes described in the articles by Pennington et al., by Cote et al., and U.S. Patent No. 5,270,264 are limited by virtue of the use of PECVD deposition, the selection of sputter gases described

15   therein, and the process parameters defined for the sputter etch step. As a result, the processes described in these references cannot be used to fill gaps having aspect ratios greater than about 2:1 and width less than about 0.65 μm (6500 Å).

20   High density plasma (HDP) chemical vapor deposition (CVD) processes are currently used to fill gaps having aspect ratios of about 3:1 and having close spacing, e.g. about 0.25 μm. HDP processes operate at a pressure regime several (e.g., two to three) orders

25   of magnitude lower than that of their PECVD counterparts. Moreover, in an HDP reactor, power is coupled inductively to the plasma, resulting in higher plasma density. Consequently, in an HDP reactor, because of the pressure and plasma characteristics, the

30   species impinging on the depositing film surface are much more energetic than in a PECVD reactor, such that gas-solid collisions may result in sputtering of the deposited film. In an HDP CVD deposition process, the

sputter etch component is typically between 10% and 20% of the net deposition rate. Another characteristic of HDP deposition is that increased bias power applied to the wafer results in an increased in-situ sputter etch

5   component, thereby decreasing the deposition rate.

By contrast, in PECVD reactors the coupling is capacitive, resulting in much lower plasma density. The combination of low plasma density and high pressure results in negligible film sputtering in PECVD

10   deposition. In addition, those skilled in the art will understand that the rate of film deposition in PECVD processes may increase with the amount of bias power applied to the wafer.

The differences in the physics and chemistry of

15   PECVD and HDP processes result in significant differences in the growth of the deposited film. In PECVD processes, plasma is used to generate deposition precursors, which in turn, are driven to the wafer surface by applied bias to the wafer. Because of the

20   relatively high pressure of operation (on the order of 1 Torr), the ions experience a large number of collisions as they cross the sheath. As a result, the flux of deposition precursor species to the wafer surface is distributed. Moreover, the mixture is

25   depleted of deposition precursors as it diffuses towards the bottom of the trench, and, as a result, the net rate of film growth at the bottom of the trench is smaller than that at the entry region of the trench. Therefore, void-free filling of gaps having high aspect

30   ratios (i.e., aspect ratios approaching or exceeding 2:1 at 0.65 μm spacing) cannot be achieved using PECVD methods since the opening to the gap will be closed long before the gap is filled. For these reasons, the process sequence described in U.S. Patent No. 5,270,264

of PECVD deposition, argon sputter etch, followed by another PECVD deposition, cannot provide void-free filling of high aspect ratio gaps at current microelectronic dimensions.

5   Existing HDP deposition processes typically employ chemical vapor deposition (CVD) with a gas mixture containing oxygen, silane, and inert gases, such as argon, to achieve simultaneous dielectric etching and deposition. In an HDP process, RF bias is applied to a

10   wafer substrate in a reaction chamber. As a result, the flux of deposition precursors is perpendicular to the wafer, and the net film growth occurs perpendicularly to the bottom of the feature. Some of the gas molecules (particularly argon) are ionized in

15   the plasma and accelerate toward the wafer surface when the RF bias is applied to the substrate. Material is thereby sputtered when the ions strike the surface. As a result, dielectric material deposited on the wafer surface is simultaneously sputter-etched to help keep

20   gaps open during the deposition process, which allows higher aspect ratio gaps to be filled.

       Figs. 1A-1D illustrate, in more detail, the simultaneous etch and deposition (etch-dep) process described above. In Fig. 1A, a gas mixture of silane

25   (SiH$_4$), oxygen (O$_2$), and an inert gas such as argon (Ar) begins depositing SiO$_2$ on the surface of a wafer 100 for filling a gap 110 between circuit elements 120. As SiO$_2$, formed from the SiH$_4$ and O$_2$, is being deposited, charged Ar and other charged ions impinge on the SiO$_2$ or

30   dielectric layer 125, thereby simultaneously etching the SiO$_2$ layer. However, because the etch rate at about 45° is approximately three to four times that on the horizontal surface, approximately 45° facets 130 form at

the corners of elements 120 during the deposition process, as shown in Fig. 1B. Figs. 1C and 1D show the process continuing to fill gap 110 with simultaneous etching and deposition of SiO_2.

In Figs. 1A-1D, the etch/dep ratio, defined as the ratio of etch rate to deposition rate, is optimized such that facets 130 remain at the corners of circuit elements 120 throughout the HDP deposition process. However, as shown in Fig. 2A, if the etch/dep ratio is decreased, facets 130 begin moving away from the corners of elements 120, and cusps 210 begin to form around the entry or opening of gap 110. Cusp formation is due in part to some of the etched SiO_2 being redeposited on opposing surfaces through line-of-sight redeposition, even though most of the etched SiO_2 is emitted back into the plasma and pumped out of the reaction chamber. This redeposition increases as the distance between opposing surfaces decreases. Therefore, as facets 130 move away from the corners of elements 120, the line-of-sight paths are shortened, resulting in increased sidewall redeposition. At a certain point in the process, cusps 210 will meet and prevent further deposition below the cusps. When this occurs, a void 220 is created in dielectric layer 125, as shown in Fig. 2B. Thus, cusp formation creates reentrant features, i.e., the width at the entry to the gap is smaller than the width at the bottom of the gap, which makes void-free gap-filling harder to achieve. The likelihood of creating voids is increased when elements 120 are reentrant before the gap-fill process begins.

On the other hand, if the etch/dep ratio is increased, as shown in Fig. 3, the etching component can etch or "clip" material from the corners of

elements 120, thereby damaging elements 120 and introducing etched contaminants 310 into dielectric layer 125.

By optimizing the etch/dep ratio, gaps with aspect
5   ratios of up to about 4:1 and widths as low as 0.15 μm can be filled without voids. However, as shown in Fig. 4, filling higher aspect ratio gaps and/or narrower widths results in voids 410 due to cusps 420 prematurely closing the gaps even if the etch/dep ratio
10   is optimized. As discussed above, this is due mainly to the shortened line-of-sight path between opposing sidewalls. Cusp formation at the entry region of high aspect ratio gaps and narrow widths to be filled cannot be totally eliminated because sputtering and
15   redeposition reactions are inherent to the physics and chemistry of the HDP CVD process. If the etch rate is increased to keep the gaps open longer, undesirable corner clipping can occur.

Therefore, with circuit densities increasing, a
20   method is desired to fill higher aspect ratio gaps with narrow widths and gaps between reentrant elements without the problems discussed above with current HDP deposition processes.

25   SUMMARY OF THE INVENTION

In accordance with the present invention, a high aspect ratio gap-fill process uses a high density plasma (HDP) deposition process with a sequence of deposition and etching steps, where the etching steps
30   utilize hydrogen (H_2) to chemically etch the deposited material.

In one embodiment, gap-fill material, such as silicon dioxide, is deposited in a gap with a deposition process in a first step of the HDP process.

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Before the entry to the gap closes, the deposition step is interrupted to prevent void formation within the gap. In the next step, the overhang or cusp is removed by chemical etching using H_2 (i.e., in a hydrogen-based plasma). The etching can be performed on an unbiased and unclamped wafer, in which case argon (Ar) gas can also be used, or with a bias HF power applied in which Ar is not used. Before the corners of the elements forming the gap are exposed from the etch step, the etch step is stopped to prevent corner clipping. Since the thickness of the material deposited at the entry region of the gap is lower than that at the bottom of the gap, the aspect ratio of the gap at the end of a deposition/etching cycle (deposition step followed by an etch step) is typically lower than the initial or previous aspect ratio. The deposition and etch steps can be repeated until the resulting aspect ratio is low enough to allow void-free gap-fill with a deposition step or a normal HDP CVD process. In principle, the overall process consists of $2n+1$ steps, where n is a positive integer.

The etching steps utilize hydrogen. However, because hydrogen is an ineffective sputtering gas (i.e., due in part to its low weight), the etching is primarily due to a chemical reaction ($SiO_2 + 2H_2 \rightarrow SiH_4 + O_2$). The etch rate increases with the LF power (or wafer temperature). Etching using this chemical reaction allows accurate control of the etch rate (due in part to a much lower etch rate than with conventional fluorine-based etch processes), a clean etching process (with no solid residual material), and high degrees of repeatability.

Throughput is also increased because the entire gap-fill process is performed in a single process

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chamber, instead of separate deposition and etch chambers. Etch/dep ratio is varied and transitions from deposition to etching steps are effected by changing the gas mixture chemical composition, the

5 power supplied to the reactor, the chamber pressure, and/or the wafer temperature.

Accordingly, this invention accomplishes void-free gap-fill for gaps having high aspect ratios (> 3.5:1) and small openings (< 0.13 μm) through use of a

10 composite multi-step HDP-CVD process using hydrogen in a chemical etch process.

This invention will be more fully understood in light of the following detailed description taken together with the accompanying drawings.

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BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1A-1D are sequential views of a conventional HDP deposition process with optimized etch/dep ratios;

Figs. 2A-2B are sequential views illustrating void

20 formation when the etch/dep ratio decreases using a conventional HDP process;

Fig. 3 is a picture of "clipped" corners when the etch/dep ratio increases using conventional HDP processes;

25 Fig. 4 is a picture of void formation when filling a high aspect ratio gap using a conventional HDP process;

Figs. 5A-5C are sequential views of high aspect ratio gaps filled with the method of the present

30 invention;

Fig. 6 is a graph showing the dependence of etch rate on LF power;

Fig. 7 is a graph showing the dependence of etch rate on LF power and wafer temperature for different dielectric materials;

Fig. 8 is a graph showing the dependence of etch rate on hydrogen pressure for different LF power levels; and

Fig. 9 is a graph showing aspect ratio as a function of the percentage of gap fill.

Use of the same reference numbers in different figures indicates similar or like elements.

DETAILED DESCRIPTION

The present invention provides a high density plasma (HDP) process using multiple sequential deposition and etch steps to fill high aspect ratio gaps, where the etch steps utilize hydrogen (H_2) to chemically etch the deposited material. Steps with etch/dep ratios less than one (referred to hereinafter as deposition steps) are used to primarily fill the gaps, while etch steps using H_2 are used to primarily open up the entries to the gaps.

The following description illustrates the use of undoped silicon oxide (USG) in filling structures of high aspect ratio (> 3.5:1) and width smaller than 0.13 μm. The shallow trench isolation (STI) step is one example for which the method of the present invention can be implemented. However, the method of the present invention can also be used in other steps in the production of integrated circuits where films are deposited, such as pre-metal dielectric (PMD) and inter-metal dielectric (IMD) films. Depending on the production step, the deposited film can be USG, phosphorus-doped oxide (PSG), fluorine-doped oxide (FSG), boron-doped oxide (BSG), boron/phosphorus doped

oxide (BPSG), and silicon-oxycarbide (SiCOH). Those
skilled in the art will thus appreciate that the use of
dopant sources, such as, but not limited to, phosphine
(PH_3), silicon tetrafluoride (SiF_4), and organosilicon

5   compounds, for deposition of these other films is
within the scope of this invention. Note that these
compounds are given as examples. The scope of this
invention is not material-specific, but it encompasses
any material which can be deposited and etched.

10   Figs. 5A-5C show the steps for one embodiment of
the present invention for filling a high aspect ratio
gap with a SiO_2 or dielectric layer 525. In Fig. 5A,
high aspect ratio gaps 510 (i.e., typically having
aspect ratios greater than 3.5:1) are formed between

15   circuit elements 520 on a substrate or wafer 100.
Circuit elements 520 can include, for example,
transistors, conductors, or interconnects. Gap 510 is
filled using an HDP process having an etch/dep ratio
less than one. Cusps 530 begin to form at the corners

20   of circuit elements 520 as SiO_2 layer 525 fills gap 510,
as shown in Fig. 5A. Before cusps 530 close the entry
to gap 510, the deposition step is stopped.
Preferably, the deposition step is stopped before the
entry to gap 510 closes. After this initial deposition

25   step, gap 510 is partially filled and partially closed.
In Fig. 5B, the next step of the HDP process uses
an chemical etch step with hydrogen to widen the entry
to gap 510. The etch step removes the cusp material
530 and, as a result, the entry to gap 510 is widened.

30   Before the corners of elements 520 are exposed, the
etch step is stopped to prevent clipping. Since the
thickness of the material deposited at the entry region
of the gap is lower than that at the bottom of the gap,
the aspect ratio of the gap at the end of the

deposition/etching cycle (a deposition step followed by an etch step) is lower than the initial or previous aspect ratio of the feature. The deposition/etching cycle is repeated as many times as necessary until the

5   resulting gap can be filled by a conventional HDP deposition step (Fig. 5A) without void formation, as shown in Fig. 5C. The material deposited during different deposition steps need not be necessarily the same. Deposition of composite structures, including,

10   but not limited to USG/PSG/USG or USG/FSG/USG, in which the overall layer consists of segments having different chemical composition, is within the scope of this invention.

Factors dictating the optimum etch/dep ratio of

15   each deposition step include the aspect ratio of the gaps and the size of the gap openings prior to each deposition step. Data from simulations and experiments can be used to maximize gap-fill process efficiency by varying the etch/dep ratio and deposition step duration

20   according to specific wafer parameters prior to each deposition step. Methods to vary the etch/dep ratio are well-known in the art and include changing the chemical composition of the reactive gas mixture, the power supplied to the wafer, the pressure of the

25   process chamber, and the temperature of the wafer. For example, increasing the HF power to the wafer, reducing the amount of silane in the gas mixture, and increasing the temperature of the wafer are some ways to increase the etch/dep ratio.

30   Table 1 provides typical process parameter ranges for a deposition step to fill a high aspect ratio gap with undoped silica glass. The gas mixture comprises oxygen and silane, and in some embodiments, also an inert gas, such as Ar or He. Low frequency power (LF)

requirements range from 2 kW to 10 kW, and high
frequency (HF) (bias) power ranges from 0.5 kW to 10
kW, dependent upon the wafer size (200 or 300 mm
diameter) and the process being used. The deposition
5   step can be performed in conventional HDP CVD reactors,
such as the standard HDP chamber (SPEED) of Novellus
Systems, Inc. of San Jose, CA. For example, in the
Novellus reactor, LF power is applied to the dome of
the reactor to create the background plasma, and HF
10   power is applied to the electrostatic chuck (ESC) to
attract ionized molecules in the plasma toward the
wafer surface for sputtering.

PROCESS PARAMETER	RANGE
Low Frequency Power (kW)	2-20
High Frequency Power (kW)	0.5-10
Chamber Pressure (mTorr)	1.5-25
Deposition Step Duration (s)	5-500
Oxygen Flow Rate (sccm)	10-1000
Inert Gas Flow Rate (sccm)	0-1000
Silane Flow Rate (sccm)	10-250

Table 1

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Note that the inclusion of other carrier and/or
reactant gases in the mixture during the USG deposition
is within the scope of this invention.

        The etch rate and duration of the H_2 etch steps is
20   optimized based on the geometry of the structure and
the topography of the cusp or overhang. The duration
of the etch steps is determined by the rate of material
removal. Data from simulations and experiments on both
monitor (flat) and structured wafers can be used to

optimize the etch step duration for each etch step in a gap-fill process.

Table 2 provides typical process parameter ranges during an etch step using hydrogen for undoped silica glass deposition. The reactive mixture will provide a non-fully directional etch in order to remove material from the side-walls of the trench and the field area. Unlike the conventional oxide etch steps described in the articles by Cote et al., Pennington et al., and U.S. Patent No. 5,270,264, the present invention relies on chemical, i.e., isotropic, etch by hydrogen to remove material from the side-walls and the entry region of the trench. Better process control is achieved through lower etching rates (discussed in more detail below). During the etch steps, the LF power varies from 1-20 kW and the HF power varies from 0-5 kW, depending on wafer size (e.g., 200 or 300 mm diameter) and the specific process requirements.

PROCESS PARAMETER	RANGE
Low Frequency Power (kW)	1-20
High Frequency Power (kW)	0-5
He Backside Pressure (Torr)	0-12
Chamber Pressure (mTorr)	5-500
Etch Step Duration (s)	5-1700
Oxygen Flow Rate (sccm)	0-500
Hydrogen Flow Rate (sccm)	100-5000
Argon Flow Rate (sccm)	0-200

Table 2

Because hydrogen is a very low weight gas, it is ineffective as a sputtering agent, such as compared with argon. However, the use of hydrogen during the

etch step is not for a physical etch, but for a
chemical etch. The energy needed for the chemical
reaction is provided by the plasma. The chemical
reaction is given by the following:

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$$SiO_2 + 2H_2 \rightarrow SiH_4 + O_2$$

As seen, the hydrogen reacts with the deposited silicon
oxide to create silane and oxygen, which is the reverse
10   of the reaction to deposit the silicon oxide from a
silane and oxygen reaction. Thus, the deposited
silicon oxide is etched away chemically, with only
silane and oxygen as by-products. However, the
chemical etch rate is much slower than conventional
15   etch processes, such as fluorine-based etches. For
example, fluorine-based etch processes can etch at
rates greater than 1 kÅ/min, while in the case of a
hydrogen-based chemical etch, the rate can be
controlled to the order of 100 Å/min. This slow etch
20   rate provides the advantage of being able to accurately
control the etch rate during the etch steps.
        The hydrogen etch of the present invention does
not exhibit loading and process drift effects between
wafers, as is common with fluorine-based etch
25   processes, thereby allowing high repeatability between
applications. Additionally, use of H_2 for etching the
overhang prevents the incorporation of
dopants/impurities (such as fluorine) into the film,
thus improving its properties and performance.
30   The etch rate for an etch step can be varied or
optimized by changing different process parameters.
Figs. 6-8 are plots showing etch rate dependence on
various parameters. Figs. 6-8 are for an unbiased,
unclamped wafer. Fig. 6 shows the dependence of etch

rate on the LF power. As seen, as the LF power increases, the etch rate increases (approximately linearly from 45 Å/min to 120 Å/min). In Fig. 7, the larger plot shows the natural log (ln) of the etch rate

5   as a function of temperature (inverse) for different types of oxides. As temperature increases (from right to left), the etch rate increases. The smaller plot at the lower left hand portion shows wafer temperature as a function of LF power. This shows that as LF power

10   increases, the wafer temperature increases. Consequently, etch rates using H_2 can be increased by increasing the LF power or temperature. This is also shown in Fig. 8. Further, in Fig. 8, the etch rate is shown as a function of H_2 pressure for different LF

15   powers. In general, the higher the H_2 pressure, the higher the etch rate.

      Optimum process results are obtained when the etching is not fully directional, i.e., etching does not occur only in the vertical direction as in the

20   processes described in the articles by Cote et al., Pennington et al., and U.S. Patent No. 5,270,264. Fully directional etching is undesirable because the process of removing cusps from the gap opening can result in the erosion of features which are located at

25   the corners of the gaps to be filled, i.e., "corner clipping." For example, in Fig. 2A, in order to remove cusps 210, the etch step, if fully directional, would have to remove an amount of material equal to the vertical height of the cusps. However, the etch step

30   would then also etch away a part of the corner of element 120. When the etch step is not fully directional (i.e., isotropic or partially isotropic), etching occurs in the horizontal directional as well, so that cusps can be removed without clipping the

corners of the elements. Thus, the range of operating pressures and the power levels used in the etching steps are chosen to satisfy this requirement. For example, unbiased (HF power = 0) conditions allow argon

5   to be used; however, with biasing (HF power > 0), argon is not used in order to avoid directional sputtering. Wafer temperature can be modulated either by clamping the wafer on the electrostatic chuck (ESC) and cooling the wafer using He or by using a heated ESC.

10   The deposition and etch steps are preferably carried out in the same process chamber, such as the Novellus SPEED reactor, and transitions from a deposition to an etching step are effected by varying the composition of the mixture, the power supplied to

15   the wafer, the chamber pressure, and/or the temperature of the wafer. Therefore, a higher throughput is possible than with processes using cluster tools, as in the processes described in the articles by Cote et al., Pennington et al. and U.S. Patent No. 5,270,264, i.e.,

20   having separate deposition and etching chambers because the wafer does not need to be transferred back and forth between two separate chambers. Furthermore, the present invention allows a cleaner and more accurate control of the etch step with greater repeatability

25   than other sequential deposition/etching methods, such as disclosed in U.S. Pat. No. 6,030,881 to Papasouliotis et al., which is incorporated by reference. By optimizing the etch/dep ratio and duration of each step, gap-fill capability and

30   throughput can be maximized, and features with aspect ratios approaching and exceeding 3.5:1 and initial opening widths narrower than approximately 0.13 μm can be filled without void formation, even when they are reentrant.

To illustrate the evolution of a structure as a
function of process time and cycles, detailed
measurements are given in Table 3 below for a structure
of 13000 Å initial spacing and with aspect ratio 4:1.
5   Fig. 9 is a graph showing the reduction of aspect ratio
as a function of the percentage of gap fill. As seen
from Fig. 9, the aspect ratio of the structure
decreases as the gap is filled. After the aspect ratio
is reduced to below 3:1, the gap can be fill completely
10   with a final deposition step.

	Bottom growth	HDP hat height	Side wall growth	Aspect ratio
After one etch/dep cycle	943 Å	970 Å	111 Å	3.74:1
After two etch/dep cycles	1665 Å	970 Å	153 Å	3.32:1
After three etch/dep cycles	2358 Å	970 Å	277 Å	2.85:1

Table 3

The above-described embodiments of the present
15   invention are meant to be merely illustrative and not
limiting. It will thus be obvious to those skilled in
the art that various changes and modifications may be
made without departing from this invention in its
broader aspects. Therefore, the appended claims
20   encompass all such changes and modifications as fall
within the true spirit and scope of this invention.